Auxiliary Chips Test Results

Cristian Gingu, Boris Baldin
Fermi National Accelerator Laboratory, Batavia, IL 60510
- January 2006 -

Introduction

This document describes test results of the auxiliary chips for CMS Forward Pixel detector: RESET, GATEKEEPER, FANOUT and FANIN chips. These chips were not tested previously on wafer. All packaged chips belong to the TBM05 batch of five wafers tested in September 2005 (see doc#467). Some potential reliability problem with this wafer batch is investigated, based on chips' failure type analysis.

1. RESET chip.

The five trays with packaged RESET chips show the following yield.

TRAY NUMBER	PASS	FAIL	TOTAL	YIELD (%)
1	69	9	78	88.5
2	75	10	85	88.2
3	77	8	85	91.6
4	71	9	80	88.7
5	71	8	79	89.9
TOTAL	**363**	**44**	**407**	**89.2**

Table 1. RESET chip yield summary.

As a general rule, the FAIL chips were tested two times only to confirm that it was not a contact problem of the chip inside the socket.

The following analog cut values were used:
01 002400 002600 'Vdig = 2.4 to 2.6 V
02 000000 000100 'Idig = 0 to 0.1 mA without CLK
03 009000 013000 'Idig = 9 to 13 mA with CLK

Note that the chip has a zero current if no CLK signal is applied to the input. A histogram of the current supply (only for the PASS chips) is presented in Figure 1.

Analysis of the FAIL defect type shows that:

1. Almost all FAIL chips have no current drawn from the 2.5V power supply and all six outputs are not passing the input signal.
2. Two of the FAIL chips behave differently. One of them has zero current supply and (only) output D is passing the input signal. The other has a current supply of ~10mA and all outputs are passing the input signal except output D.

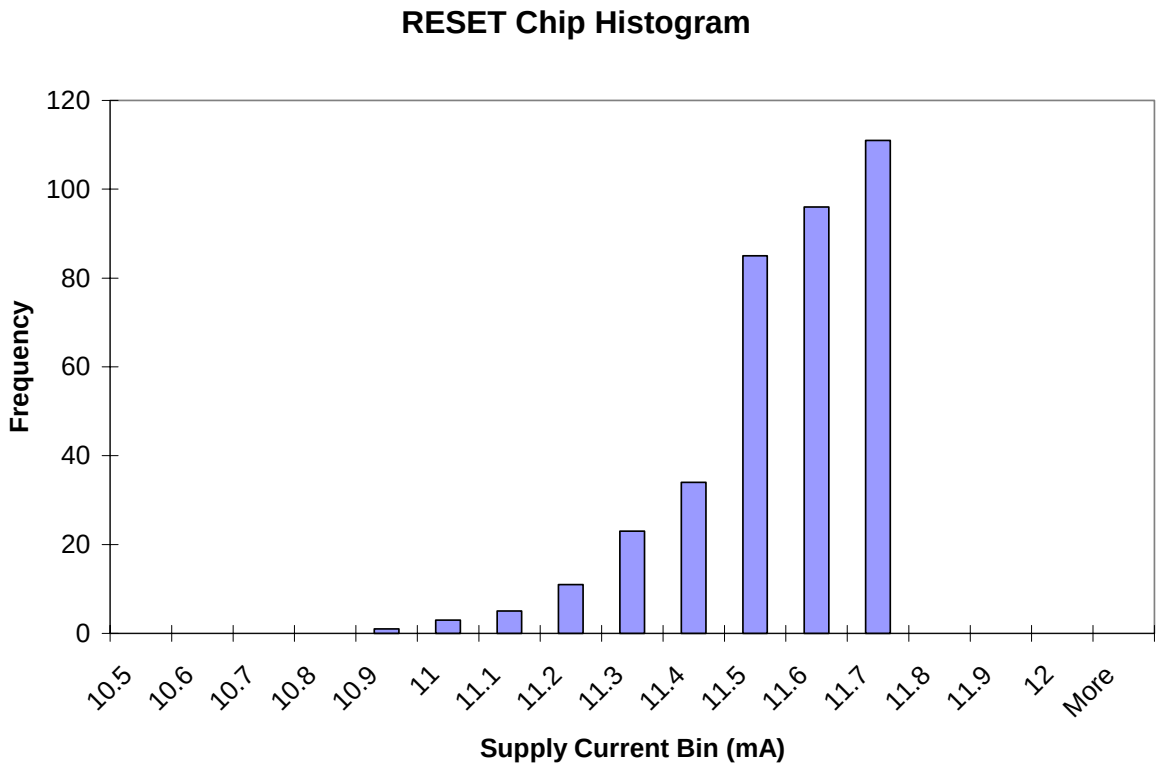

Figure 1. Supply current for the RESET chip as measured on all PASS chips.

2. GATEKEEPER chip.

The five trays with packaged GATEKEEPER chips show the following testing yield.

TRAY NUMBER	PASS	FAIL	TOTAL	YIELD (%)
1	65	17	82	79.2
2	60	19	79	75.9
3	57	19	76	75.0
4	60	23	83	72.3
5	65	15	80	81.2
TOTAL	**307**	**93**	**400**	**76.7**

Table 2. GATEKEEPER chip yield summary.

As a general rule, the FAIL chips were tested two times only to confirm that it was not a contact problem of the chip inside the socket.

The following analog cut values were used:

```
01 002400 002600   'Vdig   = 2.400 to 2.600 V
02 007000 010000   'Idig    = 7.000 to 10.000 mA without CLK
03 009000 012000   'Idig    = 9.000 to 12.000 mA with CLK
04 000100 000250   'one count in delay adjustment = 100mV to 250mV
```

The current supply was measured in two conditions (see Figure 2):

1. After power on, with no dynamic signals applied to any inputs.
2. After applying a CLK signal at CLK input and issuing a chip reset.

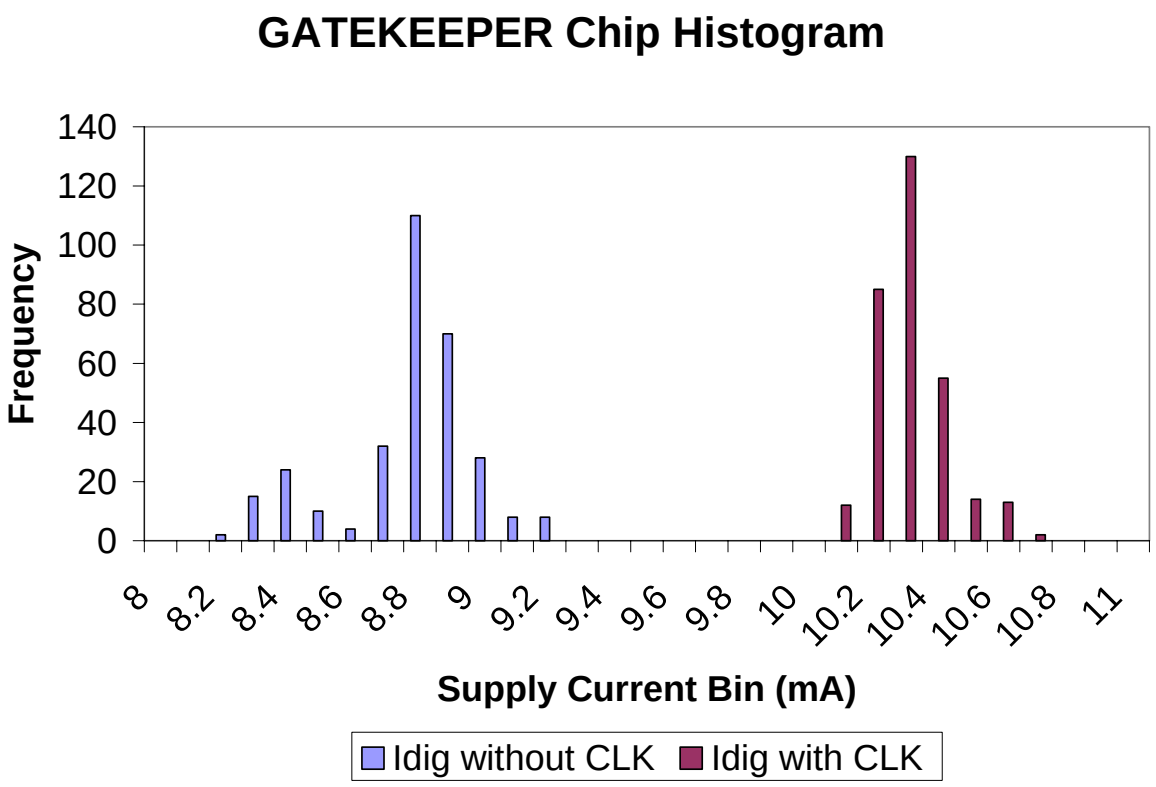

Figure 2. Supply current for the GATEKEEPER chip as measured on all PASS chips.

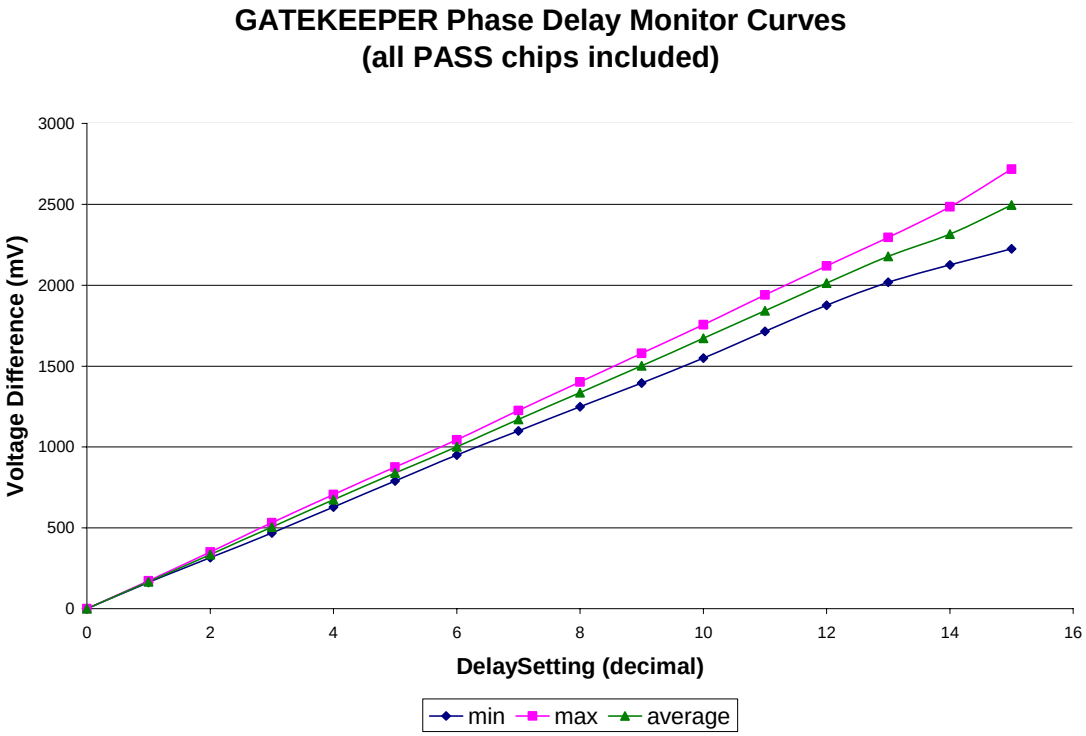

Figure 3. Phase delay monitor for the GATEKEEPER chip.

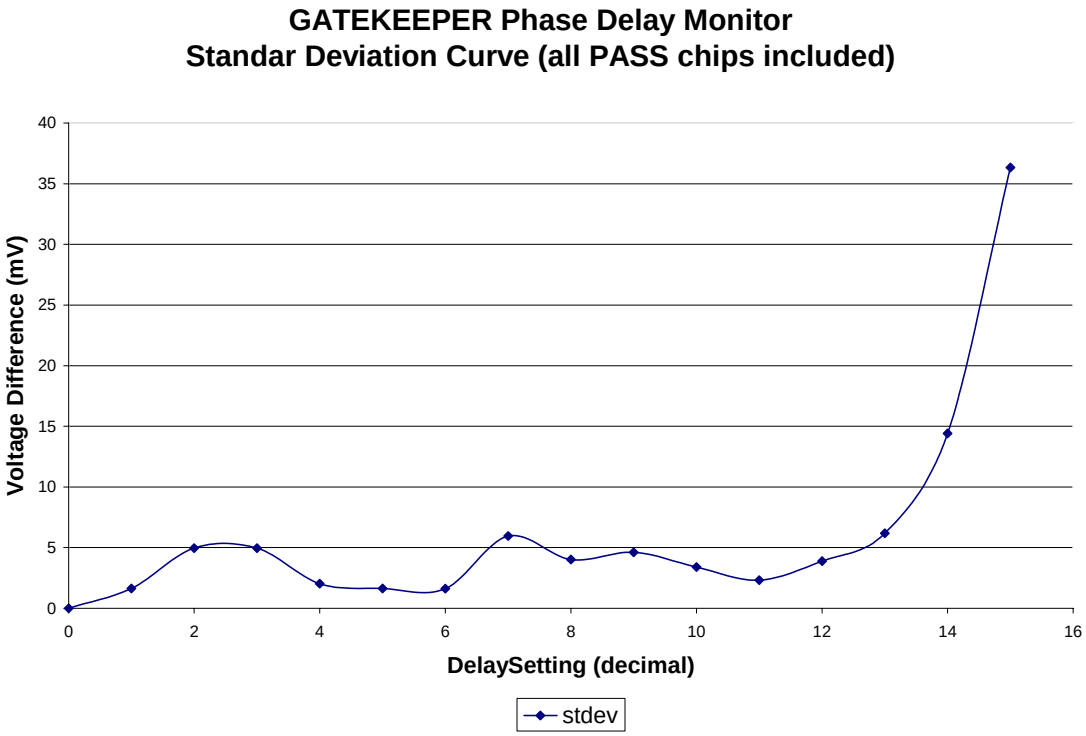

Figure 4. Phase delay monitor for the GATEKEEPER chip.

The returned CLK signal can be delayed with a programmable amount set from 0 to 15 (decimal) with one increment corresponding to 1.2ns for a total delay of 18ns. The (time) difference between sent clock and returned clock signals is converted to a DC voltage by a phase detector circuit on the test board. Measurement results for all PASS chips are presented in Figure 3, where the voltage corresponding to 0 delay setting was subtracted. The minimum, maximum and average voltage difference of all PASS chips is presented. Good linearity of the measurements can be observed. We can see also that the slope (of all PASS chips) varies from 2225mV/18ns=124mV/ns (minimum curve) to 2717mV/18ns=151mV/ns (maximum curve) with an average value of 139mV/ns.

Figure 4 shows standard deviation of the differences between two consecutive delay settings is less than ~6mV for all settings except for the last two values: 14 and 15. This is due to limitations of the measurement circuit: when the time difference between the two CLK signals becomes comparable with the rise and fall times of the signals, the linearity is affected (bandwidth limitation). Despite this fact, we consider, though, that the measurement is precise enough for our testing purpose.

An analysis of the FAIL defect type shows that about half (79) of the FAIL chips have a current supply of 0mA. The other half (83) FAIL in different modes, as shown in Table 3. On each tested chip, the tests listed in Table 3 are exercised regardless of the PASS / FAIL result on previous tests. The table shows how many times each particular test failed (remember that 79+83=162>>93 FAIL chips from Table 2 because they were measured more than just one time). A FAIL chip can FAIL one or more of the seven tests listed in Table 3. This is shown by the histogram in Figure 5. We can see that, surprisingly, the number of chips that have just one test FAIL is much larger than the chips which fail 2, 3, 4, 5, or 6 tests. None of the chips is failing all 7 tests. A closer investigation of the chips that failed only one test shows that 41 out of 52 failed on same test, the trigger path test. This rise the question why this test is more prone to failure compared with the other tests? Also, like for the RESET chip, we wonder why the power supply current test failure shows only open circuits (zero current) and not also some short circuits (high current). This might correlate with the warning of the packaging company about discolored pads on these chips and asked for our OK to proceed with packaging. It is possible that the discolored pad, which generally means the presence of an aluminum (oxide or hydroxide) compound inside the pad, made the wire bonding not reliable, perhaps lifted during package injection. One may suspect also a pad corrosion mechanism. We suggest further investigations to check the reliability of all circuits present on this wafer batch, for example a burn-in at high humidity and temperature and then retesting the chips. This reliability test should be done on all four circuits since they belong to same wafer batch.

On the other hand, all four circuits show reasonable high package yield and from this point of view it might be that there is no (hidden) reliability issue, it’s just that (from unknown reason) each circuit type is more susceptible to fail some tests.

Test description	Number of failures
Power supply current test	8
Reset path test	20
Trigger path test	43
Clock path test	10
Delay measurement test	30
Serial data path test	31
Return clock path test	25

Table 3. GATEKEEPER test failure type for chips with supply current <>0mA.

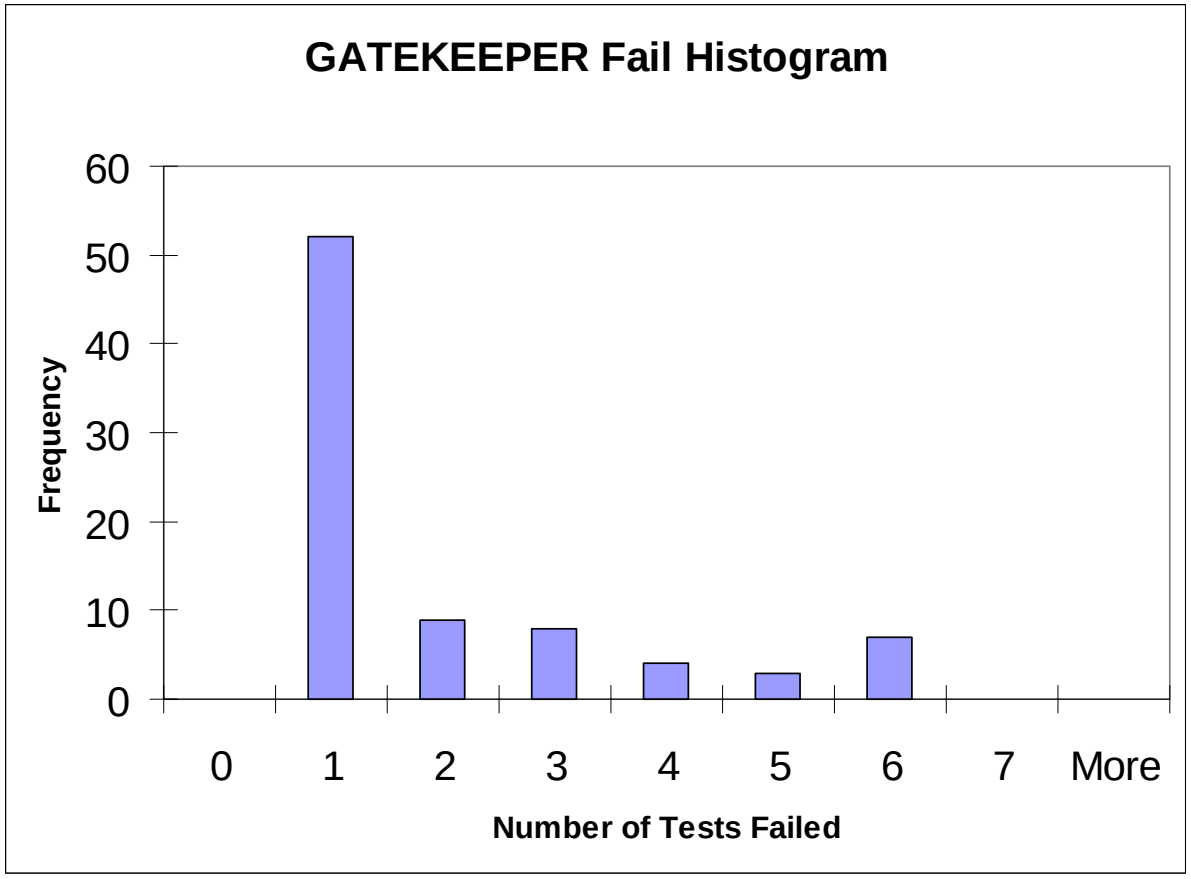

Figure 5. Number of GATEKEEPER chips that failed the tests listed in Table 3.

3. FANOUT chip.

The five trays with packaged FANOUT chips show the following yield.

TRAY NUMBER	PASS	FAIL	TOTAL	YIELD (%)
1	70	7	77	90.9
2	68	9	77	88.3
3	62	7	69	89.8
4	74	10	84	88.1
5	66	7	73	90.4
TOTAL	**340**	**40**	**380**	**89.4**

Table 4. FANOUT chip yield summary.

The following analog cut values were used:

```
01 002400 002600   'Vdig   = 2.400 to 2.600 V
02 018000 024000   'Idig   = 18.000 to 24.000 mA without CLK
03 018000 024000   'Idig   = 18.000 to 24.000 mA with CLK
```

The current supply histogram for all PASS chips (no CLK signal is applied to the input) is presented in Figure 6.

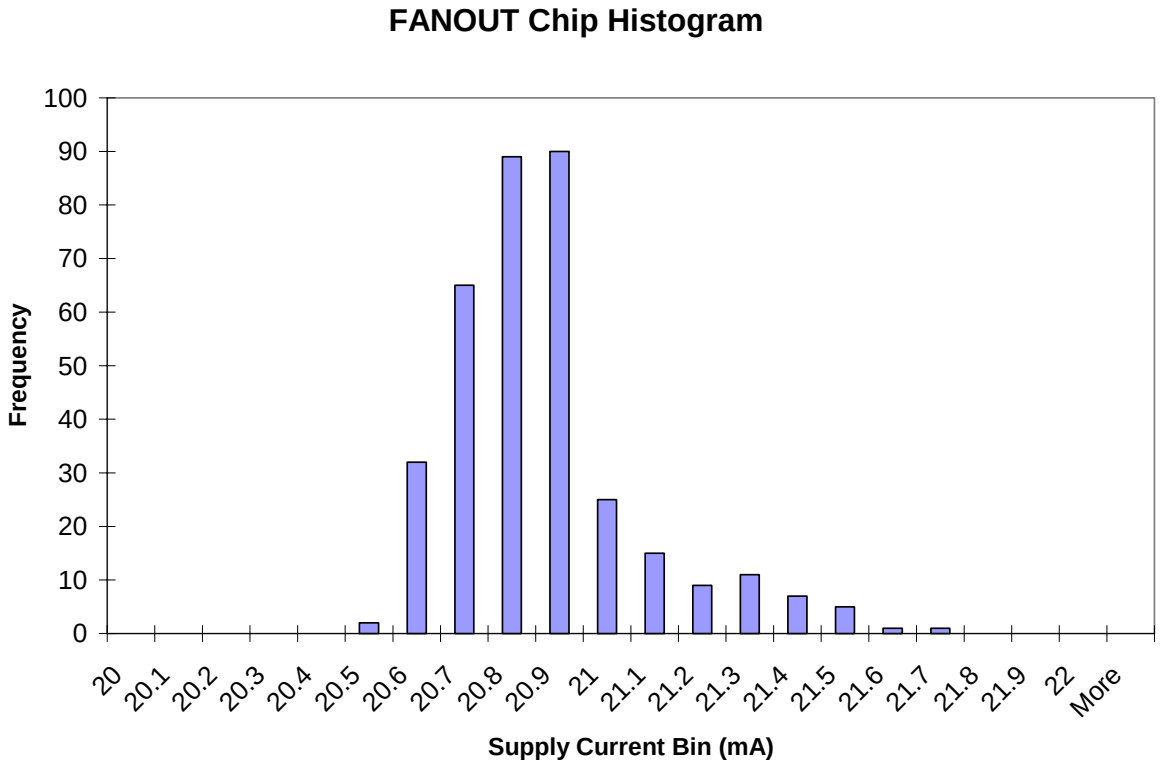

Figure 6. Supply current for the FANOUT chip as measured on all PASS chips.

An analysis of the FAIL defect type shows that:

1. All 68 FAIL chips have zero current drawn from the 2.5V power supply.
2. All 68 FAIL chips are passing the CLK input signal to outputs B and E and are not passing the CLK input signal to outputs A, C, D and F.
3. For 9 of the FAIL chips, the CLK input signal is also passing to output F.

This defect type also raises similar questions as for the other two chips: why we see only zero (open circuit) supply currents and not also some high currents (short circuit) and also what makes outputs A, C and D different from outputs B, E and F. One can only suspect either the same reliability problem or

4. FANIN chip.

The five trays with packaged FANIN chips show the following testing yield.

TRAY NUMBER	PASS	FAIL	TOTAL	YIELD (%)
1	69	8	74	89.6
2	74	11	85	87.0
3	74	9	83	89.1
4	71	9	80	88.7
5	74	10	84	88.1
TOTAL	**362**	**37**	**406**	**89.1**

Table 5. FANIN chip yield summary.

The following analog cut values were used:

```
01 002400 002600   'Vdig   = 2.400 to 2.600 V
02 005500 007500   'Idig   = 5.500 to 7.500 mA without CLK
03 005500 007500   'Idig   = 5.500 to 7.500 mA with CLK
```

The current supply histogram for all PASS chips (no CLK signal is applied to the input) is presented in Figure 7.

An analysis of the FAIL defect type shows that:

1. From the total of exactly 47 FAIL chips, 44 have zero current drawn from the 2.5V power supply.
2. The other 3 fail in two modes: two of them are not passing at all the input CLK signal and one of them fails only on two inputs (A and B).

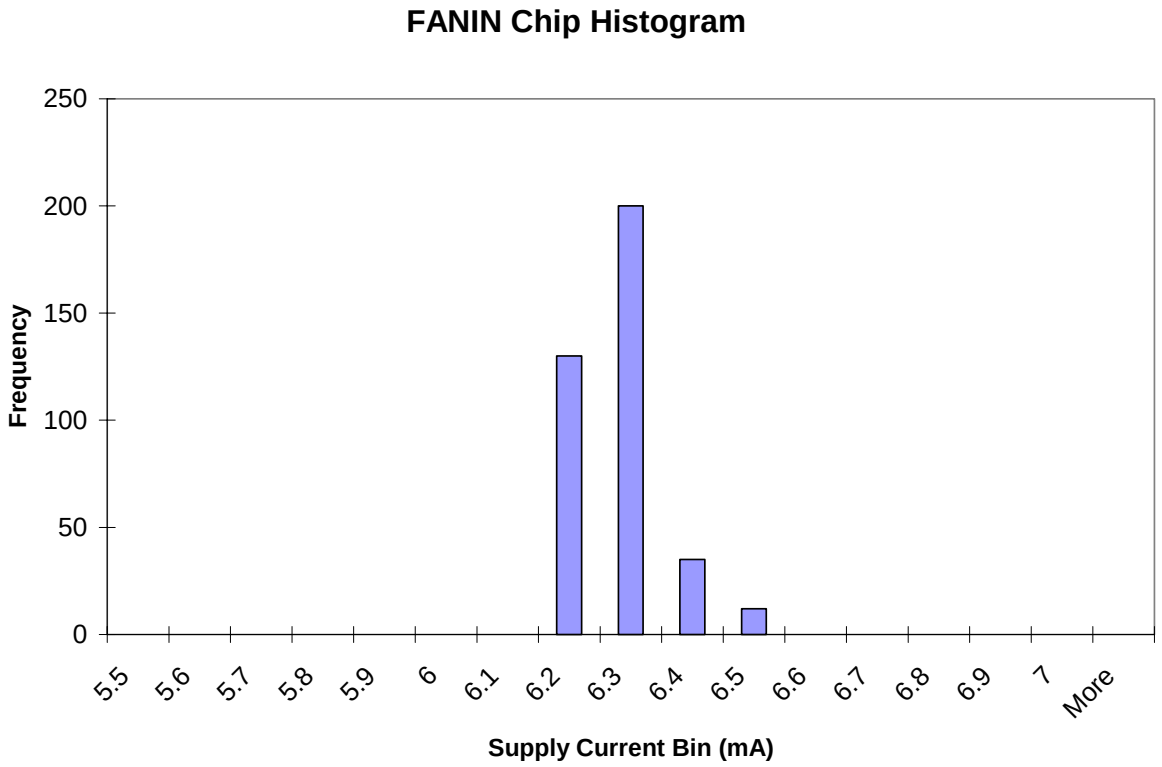

Figure 7. Supply current for the FANIN chip as measured on all PASS chips.

Conclusions

The test results of the auxiliary chips for CMS Forward Pixel detector (RESET, GATEKEEPER, FANOUT and FANIN) were presented. All packaged chips (wafers) show relatively high yield, from 87% to 91% with the exception of the GATEKEEPER which shows a lower yield, from 72% to 81%. A detailed defect analysis was done, suggesting either some specific failure modes or some possible reliability problems. The later is of more concern and a burn-in test is suggested and will be performed on all four types.